Customer No.: 31561
Application No.: 10/707,354
Docket No.: 10465-US-PA

REMARKS

Claims 1-5 and 7-18 are pending of which the claims 1, 5 and 7-9 have been amended and the claims 19-21 have been added without prejudice or disclaimer in order to more explicitly describe the claimed invention. Further, Figs 2 and 3 were amended due to their existing clerical errors of reference numeral, "Vin20." The formal drawings of Figs 2 and 3 will be submitted after the present invention is allowed. It is believed that no new matter is added by way of amendments made to claims, drawings and the application. For at least the foregoing reason, Applicants respectfully submit that claims 1-5, 7-9 and 11-21 patently define over prior art of record and reconsideration of this application is respectfully requested.

In the specification

Enclosed Please find two copies of the amended specification, one of which is a marked version and another is a clean version. In the marked version, to be consistent with the amended Figs 2 and 3, one of the two inputs of element 202, the label "Vin20," is amended to be "Vin21. Likewise, to be consistent with the amended claims, "push signal Vg_1," "pull signal Vg_2," "decayed push signal Vg_3"and "decayed pull signal Vg_4," were amended to be "first push signal Vg_1," "first pull signal Vg_2," "second push signal Vg_3"and "second pull signal Vg_4," respectively.

Customer No.: 31561
Application No.: 10/707,354
Docket No.: 10465-US-PA

In The Drawings

In Figs 2 and 3, as the two inputs of element 202 should not labeled with reference numeral "20, " the label "Vin20" was amended to be "Vin21,"as shown in the amended Figs 2 and 3.

Discussion for rejection to claims under 35U.S.C. 112 2nd paragraph

2. *Claims 1-18 are rejected under 35 U.S.C. 112 2nd paragraph as being indefinite for failing to particularly point out the subject matter the applicant regards as the invention.*

In response thereto, applicant appreciates the examiner pointed out the claims' indefiniteness. It is the terms of "decayed push/pull signal" that cause the claims 1-18 indefinite. Accordingly, to eliminate such indefiniteness, the terms of "decayed push/pull signal" are amended to be "second push/pull signal," as disclosed in the amended claims and a clean version of the amended specification.

Discussion for rejection to claims under 35U.S.C. 103 (a)

3.Claims 1-5,7-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over any one of Miyabi, Kogushi, Hunt, Garcia and Sanwo in view of any one of Taguchi, Taito, Morishita and Cruz.

In response thereto, applicant respectfully traverses the preceding rejection based on the following arguments. To establish a prima facie case of obviousness, the prior art references must suggest or disclose a motive (or desirability) of the present invention. Furthermore, there must be some motivations to combine the references; these motivations must come from "the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir.1998). Accordingly, to cause any one skilled in the art to which the present invention pertains to make the combination of prior art references, the primary requirement is that problems intended to be solved by each prior art reference should be explicitly or implicitly not only addressed and identical each other, but identical to that of the present invention as well.

In the first group prior art references, i.e. Miyabi, Kogushi, Hunt, Garcia and Sanwo, from their "SUMMARY OF THE INVENTION," Sanwo discloses an output buffer circuit with a controllable or programmable slew rate with an objective of preventing the large voltage drop at output terminal caused by too fast slew rate; Garcia discloses the same output buffer circuit as Sanwo, wherein the main output stage constituted by P3,N2,P2 and N3 is connected to the gate of P1 and that of N1, as well as supplies the required current of P4 and N4. In contrast, the main output stage

and assistant output stage of the present invention is connected together to drive output terminal. Moreover, Kogushi discloses an output buffer circuit with a cost reduction and a stable operation. Wherein, transistors 4-7 are connected to output through capacitor 14. In fact, transistors 10 and 11 serve as the output stage of the present invention, not an assistant output stage as alleged by the examiner. This is because reference numerals 12 and 22 are PMOS and NMOS respectively, and reference numerals 13 and 23 are NMOS and PMOS respectively. When PEN is equal to a " HIGH" level, transistors 6,10,13,22 are turned on so as to cause transistors 22,10 to supply currents Ip1,Ic1 to transistors 6 and 7 through node N1. However, due to the initial potential of the capacitor 14 and equivalent resistance of transistors 6 and 7, the discharging speed of the gate of the transistor 10 is lowered, which in turn lowers slew rate of output signal. Accordingly, the structures of the main output stage and assistant output stage are distinct from those of the invention. In Fig.6, in Miyabi, reference numerals 65,66 are referred to a delay circuit with output of either "0" or "1" logic level, which is used to delay transistors 63, 64' being turned on. Moreover, the Fig.6 has one "IN" input terminal instead of two input terminal of the invention so that Miyabi and the invention have different input terminal structures.

Additionally, Hunt discloses an output circuit with a controllable slew rate, wherein Fig.3 employs RC delay to control the speed of turning on/off of transistors

50, 54, thereby resolving the crowbar current problem occurred at simultaneously turning of transistors 50, 54. Fig.4 employs bufl-bufn to replace the resistance 60 shown in Fig.3 to control the slew rate of the output circuit.

To summarize, the input and output of the first group cited references are either "0" or "1" logic level and their objectives are control slew rate of the output buffer circuit to prevent the overlarge instantaneous current from generating power noise during the output of digital signals. However, the input and output of the invention are analog signals and the invention employs a level shifter to generate a DC voltage that allows the assistant output stage to be turned off during the main output stage's operating at a condition of a quiescent DC biased current.

In the second group prior art references, i.e. Taguchi, Taito, Morishita and Cruz, Taguchi, from their"SUMMARY OF THE INVENTION." In Cruzc, it employs L(34) and C(32) to generate resonant frequency to reduce clock jitter; in Morishita, it provides a detecting circuit for detecting external VCC and reference voltage; in Taito, there discloses a buffer circuit with an output of either "0" or "1" logic level and a potential detecting circuit for detecting input signal whether to reach a target value and if yes, output to a next stage and in Taguchi, there only discloses a peak/bottom circuit for detecting output of a laser, which totally has nothing with the invention.

In summary, the problems intended to be solved by second group prior art references are distinct from "the problem of improving slew rate," as intended to

resolve by the first group prior art references.

As stated above, to cause any one skilled in the art to which the present invention pertains to make the combination of the first group and the second group prior art references, the primary requirement is that problems intended to be solved by each group prior art reference should be explicitly or implicitly not only addressed and identical each other, but identical to that of the present invention as well. Accordingly, neither the first group prior art references, nor the second prior art references teach, suggest the desirability of making the combination. Thus, claims 1-5, 7-8 are not rendered obvious by all prior art references and accordingly patentable.

Furthermore, as to the examiner allegation that each of second group prior art references 'disclosure of a buffer coupled to a differential amplifier and replacing the buffer with that of the first group prior art references, however, the conclusion of claims' 1-5, 7-8 being rendered obvious is made based on the fact that the examiner used the claims of the present invention as a "template" to piece together the teaching of the prior art references to arrive the claims of the present invention. That is, the conclusion of claims' 1-5, 7-8 being rendered obvious is made based on impermissible hindsight. Accordingly, claims 1-5, 7-8 should not be rendered obvious based on the examiner's hindsight and accordingly patentable.

Even if the preceding two groups of references could be combined, these proposal combinations still fail to teach, suggest or disclose "A circuit for enhancing a slew rate of an operational amplifier, comprising..., the gates of the first and second field effect transistors are connected to an output of a differential amplifier and the main current further comprises a quiescent DC biased current and the push signal and the pull signal are level shifted from the output of the differential amplifier" as claimed in the amended claim 1, and" A method for enhancing a slew rate of an operational amplifier, comprising..., the gates of the first and second field effect transistors are connected to an output of a differential amplifier the second push current or the second pull current is generated as an assistant current when either the third field effect transistor with the first type is turned on or the fourth field effect transistor with the second type is turned on," as claimed in the amended claim 5. Accordingly, the amended independent claims cannot be rendered obvious by these proposal combinations and thus patentable.

Regarding dependent claims 2-4 and 7-8, they are patentable as a matter of law for the reason that they contain their corresponding patentable base claims.

4. *Claims 9-18 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112 2nd paragraph.*

Customer No.: 31561
Application No.: 10/707,354
Docket No.: 10465-US-PA

In response thereto, the claims 9-18 are so amended to meet 35 U.S.C. 112 2nd paragraph. In the amended claim 9, the terms of "decayed push/pull signal" are amended to be "second push/pull signal."

Customer No.: 31561
Application No.: 10/707,354
Docket No.: 10465-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-5, 7-9 and 11-21 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-5, 7-9 and 11-21 of the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Jan. 16, 2006

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Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

Marked Version

SLEW RATE ENHANCEMENT CIRCUIT VIA DYNAMIC OUTPUT STAGE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92105571, filed March 14, 2003.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a slew rate enhancement circuit. More particularly, the present invention relates to the slew rate enhancement circuit which is compact and occupies small chip area.

Description of Related Art

[0002] To achieve a high slew rate, when ~~the~~ an operational amplifier ("OPAMP") drives a heavy load. Many techniques are used to enhance the slew rate, such as: increasing operating current of OPAMP, reducing a compensation capacitor, or being connected to an error amplifier. Except for the high slew rate, a lot of disadvantages such as a high operating current and a stability degradation for original OPAMP, a large chip area, complexity of circuit design, noise and offset are introduced from the followed error amplifiers.

[0003] FIG. 1 illustrates a high slew rate amplifier according to a prior art. The circuit in FIG. 1 includes an OPAMP 102, error amplifiers 104, 106 and a push-pull output stage 112. The push-pull output stage includes a P-type Metal Oxide

Marked Version

Semiconductor ("PMOS") transistor 108 and an N-type Metal Oxide Semiconductor ("NMOS") transistor 110. The inverting inputs of the error amplifier 104 and the error amplifier 106 are connected to the output of the OPAMP 102 at a node N11. The non-inverting inputs of the error amplifier 104 and the error amplifier 106 are connected to a load at a node N12. The loop of connection between an output of the error amplifier 104 and the gate of the PMOS transistor 108, and the loop of connection between the drain of the PMOS transistor 108 and the non-inverting input of the error amplifier 104 formed a negative feedback loop. Likewise, the loop of connection between the output of the error amplifier 106 and the gate of the NMOS transistor 110, and the loop of connection between the drain of the NMOS transistor 110 and the non-inverting input of the error amplifier 106 also formed a negative feedback loop. The node N11 and the loop including node N12 construct a virtual short loop. The virtual short loop and both of the negative feedback loops are applied to control the PMOS transistor 108 to push current to the load or to control the NMOS transistor 110 to pull current from the load.

[0004] The error amplifier 104 and the error amplifier 106 are applied to monitor the output signals of the OPAMP 102. When a non-inverting input Vin10 is not equal to an inverting input Vout10, the error amplifier 104 and the error amplifier 106 turn on the PMOS transistor 108 to push a current to the load, or turn on the NMOS transistor 110 to pull a current from the load. On the other hand, when the signal Vin10 is equal to the signal Vout10, the PMOS transistor 108 and the NMOS transistor 110 work under the DC bias condition.

[0005] In general, the circuit of FIG. 1 is usually applied to a buffer amplifier. In order to provide a large current from the PMOS transistor 108 and the NMOS

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transistor 110, aspect ratios of the PMOS transistor 108 and the NMOS transistor 110 should be as large as possible, but a static operating current is also increased according to the aspect ratio. Furthermore, a real circuit on a chip is more complicated than FIG. 1, since the error amplifier 104 is constructed by at least 5 pieces of Metal Oxide Semiconductor ("MOS") transistors, and so dose the error amplifier 106. If the Miller Compensation is applied to compensate the pole/zero location shifts, the other two compensation capacitors are introduced into the circuit of FIG. 1. If the offset voltage, symmetry of layout, cross distortion, linearity, bandwidth and noise of and from the error amplifier 104 and error amplifier 106 are calibrated, additional circuits will be added to the circuit of FIG. 1. Therefore, the manufacturing of the circuit of FIG. 1 on a chip will occupy a huge chip area and consume a high static operating current of the original OPAMP.

SUMMARY OF THE INVENTION

[0006] As embodied and broadly described herein, the invention provides an improved circuit, denoted as a dynamic output stage for enhancing of the slew rate. The original operational amplifier includes a differential amplifier and a main output stage. The dynamic output stage includes a monitoring stage and an assistant output stage. The main output stage detects an input voltage from a differential amplifier to decide whether to output a main current to the load or not. The main output stage also generates a push signal and a pull signal for the monitoring stage. The monitoring stage decays the push signal and the pull signal, and the assistant output stage will receive the decayed push signal and the decayed pull signal to decide whether to provide an assistant current to the load or not. The assistant current is an additional

Marked Version

huge current for enhancing the slew rate. The assistant current is turned on/off automatically and will not affect the operation status of the original OPAMP and the main output stage. Furthermore, the dynamic output stage does not consume the static operating current. Compared with the error amplifiers in the prior art, this invention will not introduce the offset voltage, compensation, distortion and noise Therefore, no calibration will be needed.

[0007] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0009] Fig. 1 is a conventional high slew rate amplifier.

[0010] Fig. 2 is a sketch of the dynamic output stage of a preferred embodiment of the present invention.

[0011] Fig. 3 is a detail circuit of the dynamic output stage of a preferred embodiment of the present invention.

[0012] Fig. 4 is the graph of the final push current and the final pull current at the node N25 versus the push and pull signal of OPAMP with and without this ~~art~~ invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] FIG. 2 depicts of the dynamic output stage of a preferred embodiment of the present invention. An OPAMP includes a differential amplifier 202 and a main output stage 204. The differential amplifier has an inverting input, denoted as Vout 20 and a non-inverting input, denoted as Vin ~~20~~ 21. The output of the differential amplifier, denoted as node N21, is connected to the main output stage 204. The main output stage 204 includes a plurality of sub-circuits; which comprises a voltage source 220, a first field effect transistor (FET) with a first type, for example, a first PMOS transistor 216, a voltage source 222 and a second FET with a second type, for example, a second NMOS transistor 218. The first and second field effect transistors provide the first push current and first pull current, respectively. The output of the differential amplifier 202 is connected to the voltage source 220 and the voltage source 222 at a node N21. The drain of the first PMOS transistor 216 is connected to the drain of the second NMOS transistor 218 at a node N22. The gate of the first PMOS transistor 216 is connected with the voltage source 220 and with a voltage source 208 at a node N23. A first push signal Vg1 is generated by the main output stage 204 at the node N23 and the signal Vg1 also stands for the voltage of the node N23. The source of the first PMOS transistor 216 is connected to an input power Vdd. The gate of the second NMOS transistor 218 is connected to the voltage source 222 and with a voltage source 210 at a node N24. A first pull signal Vg2 is generated by the main output stage 204 at the node N24 and the signal Vg2 also stands for the voltage of the node N24. The source of the second NMOS transistor 218 is connected to the ground. The voltage of the voltage source 208 is V1 and the voltage of the voltage source 210 is V2. An assistant output stage 206 includes a third FET with the first type, for example, a third PMOS transistor

Marked Version

212 and a fourth FET with the second type, for example, a fourth NMOS transistor 214. The third and fourth field effect transistors provide the second push current and second pull current, respectively. The drain of the third PMOS transistor 212 is connected to the drain of the fourth NMOS transistor 214 at a node N25. The node N22 is connected to the node N25 and the load. The gate of the third PMOS transistor 212 is connected to the voltage source 208 and the gate of the fourth NMOS transistor 214 is connected to the voltage source 210.

[0014] In a steady state, the voltage Vin~~20~~ 21 is equal to the voltage Vout20, the main output stage 204 does not apply any current to the load. A second push signal, ~~decayed~~ i.e. level shifted push signal Vg3, denoting the gate voltage of the third PMOS transistor 212 is equal to the first push signal Vg1 minus the voltage V1. The voltage V1 is large enough, so the ~~decayed~~ level shifted push signal Vg3 is not able to turn on the third PMOS transistor 212. Likewise, a second pull signal, ~~decayed~~ i.e. level shifted pull signal Vg4, denoting the gate voltage of the fourth NMOS transistor 214 is equal to the first pull signal Vg2 minus the voltage V2. The voltage V2 is large enough, so the ~~decayed~~ level shifted pull signal Vg4 is not able to turn on the fourth NMOS transistor 214. No current will be applied to the load from the assistant output stage 206.

[0015] When the steady state no longer exists, the voltage Vin21 is larger than the voltage Vout20. The output node N21 of differential amplifier 202 will approach to the GND potential. The gate voltage N23 of the first PMOS 216 will approach to the GND potential, too. Thus, the first PMOS 216 will apply a main current to the load from node N22. The push signal Vg1 is fed forward to the assistant output stage 206 via the voltage source 208. The first push signal Vg1 is decayed by the voltage source 208, which results in a ~~decayed~~ level shifted push signal Vg3. This ~~result in decayed~~ level

Marked Version

shifted push signal Vg3 will approach ~~to~~ the GND potential, even though the potential voltage of Vg3 is 'Vg1+V1'. The decayed push signal is large enough to turn on the first PMOS 216. Meanwhile, the gate voltage N24 of the second NMOS 218 will approach to the GND potential, thus the second NMOS 218 is turned off. The first pull signal Vg2 is fed forward to the assistant output stage 206 via the voltage source 210. The first pull signal Vg2 is decayed by the voltage source 210, which results in a ~~decayed~~ level shifted pull signal Vg4. This ~~result in the~~ level shifted pull signal will approach the GND potential, and the fourth NMOS 214 is turned off. Therefore, the assistant output stage 206 will also apply an assistant current to the load from the node N25. When the voltage Vin21 turns into a little larger than the voltage Vout20, the gate voltage N23 of the first PMOS 216 and the gate voltage N24 of the second NMOS 218 will return to a steady state condition. Due to the voltage source 208 and 210, the assistant output stage 206 will turn off and no longer apply an assistant current to the load. The main output stage will apply current to the load until the voltage Vin~~20~~ 21 equals Vout20.

[0016] When the voltage Vin~~20~~ 21 is smaller than the voltage Vout20, the output node N21 of differential amplifier 202 will approach to Vdd. The gate voltage N24 of the second NMOS 218 will approach to Vdd, too. Thus, the second NMOS 218 will apply a main current to the load from node N22. The first pull signal Vg2 is fed forward to the assistant output stage 206 via the voltage source 210. The first pull signal Vg2 is level shifted by the voltage source 210, which results in a ~~decayed~~ level shifted push signal Vg4. This result in the ~~decayed~~ level shifted pull signal Vg4 will approach to Vdd, even though the potential voltage of Vg4 is 'Vg2+V2'. The level shifted pull signal is large enough to turn on the NMOS 214. Meanwhile, the gate voltage N23 of

Marked Version

the first PMOS 216 will approach to Vdd, thus the first PMOS 216 is turned off. The first push signal Vg1 is fed forward to the assistant output stage 206 via the voltage source 208. The first push signal Vg1 is level shifted by the voltage source 208, which results in a ~~decayed~~ level shifted push signal Vg3. This ~~result in the decayed~~ level shifted pull signal will approach to Vdd, and the third PMOS 212 is turned off. Therefore, the assistant output stage will also apply an assistant current to the load from the node N25. When the voltage Vin20 1 turns into a little smaller than the voltage Vout20, the gate voltage N23 of the first PMOS 216 and the gate voltage N24 of the second NMOS 218 will return to a steady state condition. Due to the voltage source 208 and 210, the assistant stage 206 will turned off and no longer apply an assistant current to the load. The main output stage will apply current to the load until the voltage Vin~~20~~21 equals Vout20. The novel technology presented above is the dynamic output stage.

[0017] FIG. 3 is a detail circuit of the dynamic output stage in the present invention, wherein the voltage sources 208 and 210 are replaced by a monitoring stage 302. The monitoring stage 302 includes a fifth FET with the first type, for example, a fifth PMOS transistor 304, a current source 308, a sixth FET with the second type, for example, a sixth NMOS transistor 306 and a current source 310. The gate of the fifth PMOS transistor 304 is connected to the gate of the first PMOS transistor 216 at the node N23. The source of the fifth PMOS transistor 304 is connected to the gate of the third PMOS transistor 212 and to the current source 308 at a node N26. The drain of the fifth PMOS transistor 304 is connected to the ground. The gate of the sixth NMOS transistor 306 is connected to the gate of the second NMOS transistor 218 at the node N24. The source of the sixth NMOS transistor 306 is connected to the gate of the

Marked Version

fourth NMOS transistor 214 and to the current source 310 at a node N27. The other circuit devices and connections between these devices in FIG. 3 are the same as those in FIG.2.

[0018] In FIG. 3, when the voltage Vin~~20~~21 is equal to the voltage Vout20 in the steady state, the main output stage 204 does not apply any current to the load. The first PMOS transistor 216 and the second NMOS transistor 218 will work under the quiescent current bias condition so that even a voltage at the inverting input is equal to that at the non-inverting input, there exists a quiescent DC biased current at the node N_{22}. A voltage difference between the node N26 and the node N23 will be equal to a threshold voltage Vt1 of the fifth PMOS 304 at least. Likewise, the voltage difference between the node N27 and the node N24 will be at least equal to a threshold voltage Vt2 of the sixth NMOS 306. The first push signal Vg1 is decreased by the threshold voltage Vt1, and therefore the second push signal, i.e. ~~decayed~~ level shifted push signal Vg3 will be equal to Vdd, thus the third PMOS transistor 212 will be turned off. The first pull signal Vg2 is also increased by the threshold voltage Vt2, and therefore the second pull signal, i.e. ~~decayed~~ level shifted pull signal Vg4 will be equal to the ground, thus the third NMOS transistor 214 will also be turned off. Therefore, the assistant output stage will not apply any current to the load.

[0019] When the steady state no longer exists, the voltage Vin21 is larger than the voltage Vout20, the first pull signal Vg2 will approach the ground, and therefore the second NMOS transistor 218 will be turned off. The first push signal Vg1 will approach the ground, and therefore the first PMOS transistor 216 will be turned on. The result is that the main output stage 204 pushes a main current to the load. The ~~decayed~~ level shifted push signal Vg3 is equal to the first push signal Vg1 plus the absolute value of

Marked Version

the voltage difference between the gate and the source of the fifth PMOS transistor 304. Likewise, the ~~decayed~~ level shifted pull signal Vg4 is equal to the first pull signal Vg2 minus the absolute value of the voltage difference between the gate and the source of the sixth NMOS transistor 306. Since the second NMOS transistor 218 is turned off, the fourth NMOS transistor 214 will also be turned off. The first PMOS transistor 216 is turned on, the ~~decayed~~ level shifted push signal Vg3 is able to turn on the third PMOS transistor 212 to push an external current to the load. The final result is that the assistant output stage will push an assistant current to the load. When the voltage Vin~~20~~21 turns into a little larger than the voltage Vout20, the push signal Vg1 and the pull signal Vg2 will return to a quiescent bias condition. Since Vg1 and Vg2 is level shifted by the fifth PMOS transistor 304 and the sixth NMOS transistor 306, the second push signal Vg3 and the second pull signal Vg4 will be not enough to turn on the third PMOS transistor 212 and the fourth NMOS transistor 214. Therefore the assistant output stage will not apply any current to the load. The load will be driven by the current from the main output stage 204 till the voltage Vin21 equals ~~to~~ the Vout20.

[0020] When the steady state no longer exists, the voltage Vin~~20~~21 is smaller than the voltage Vout20, the push signal Vg1 will approach to Vdd, and therefore the first PMOS transistor 216 will be turned off. The first pull signal Vg2 will approach to Vdd, and therefore the second NMOS transistor 218 will be turned on. The result is the main output stage 204 will pull a main current from the load. Since the first PMOS transistor 216 is turned off, the third PMOS transistor 212 will also be turned off. The second NMOS transistor 218 is turned on, the ~~decayed~~ level shifted pull signal Vg4 is able to turn on the fourth NMOS transistor 214 to pull an external current from the load. The final result is that the assistant output stage will pull an assistant current from the

Marked Version

load. When the voltage Vin21 turns into a little smaller than the voltage Vout20, the first push signal Vg1 and the first pull signal Vg2 will return to the quiescent bias condition. Since Vg1 and Vg2 are level shifted by the fifth PMOS transistor 304 and the sixth NMOS transistor 306, the second push signal Vg3 and the second pull signal Vg4 will be not enough for the third PMOS transistor 212 and the fourth NMOS transistor 214. Therefore, the assistant output stage will not pull any current from the load. The load will be driven by the current from the main output stage 204 till the voltage Vin21 equals the Vout20.

[0021] The assistant output stage is an apparatus, which could provide the extra current to the load. The assistant output stage is controlled by the fifth PMOS transistor 304 and the sixth NMOS transistor 306, which operate as a source follower. Thus, the assistant output stage will be turned on after the main output stage is turned on, and be turned off before the main output stage is turned off. The assistant output stage is turned on/off automatically, and furthermore the assistant output stage does not consume the static operating current. The problem of prior art such as: offset voltage, pole/zero location, and linearity, will no longer exist. The slew rate of operational amplifier is increased without consuming the extra operating current and degrades stability.

[0022] Fig. 4 is the graph of the final push current and the final pull current at the node N25 versus the push and pull signal of OPAMP with and without this invention. The final push current and the final pull current are obviously increased by the assistant output stage. In FIG.4, the push current with this invention is larger than the push current without this invention under the same push signal V01. Likewise, the pull current with this invention is larger than the pull current without this invention under the same pull signal V02. Therefore, the final push current or pull current is

Marked Version

higher for the original OPAMP with this invention. With the dynamic output stage in this invention, it is easy to enhance the slew rate without increasing static operating current of the original OPAMP.

[0023] Accordingly, the circuit and method provided in the present invention can be used to any circuit having at least two inputs, for example, a first input and a second input and a main current. The method of the invention includes that, first of all, detecting a first input and a second input. Secondly, a push current is generated when a voltage of the second input is larger than a voltage of the first input and their difference is large enough to turn on at least one of the switches. Otherwise, a pull current is generated when a voltage of the first input is larger than a voltage of the second input and their difference is large enough to turn on at least one of the switches. Thus, the push circuit and the pull circuit can be used to enlarge the main current to enhance the slew rate. Moreover, the push current and the pull current are further fed back to one of the first input and the second input. Furthermore, the push current and the pull current is turned on automatically after the main current is turned on, and is turned off automatically before the main current is turned off.

[0024] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

Marked Version

ABSTRACT OF THE DISCLOSURE

A slew rate enhancement circuit of an operational amplifier including a main output stage, a monitoring stage and an assistant output stage is provided. An input voltage of the operational amplifier is detected by the main output stage to decide whether to output a main current to the load or not. The main output stage also generates a first push signal and a first pull signal according to the input voltage, and thereafter the second push signal and second pull signal are level shifted by the monitoring stage. ~~The~~ A ~~decayed~~ second push signal and ~~decayed~~ second pull signal will turn on or turn off the assistant output stage to decided whether to output an assistant current to the load or not. Specially, the improved compact circuit does not increase static operating current for the original operational amplifier and occupy a small chip area.

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